BM1382

Bitcoin Hash ASIC Datasheet

BitMain Technologies Limited

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Revision History

Revision Number	Author	Date	Description
1.0	Zhan	2014.4	Initial
2.0	Zhan	2014.4	Change pin location
3.0	Zhan	2014.6	Add work input timing

1Overview

BM1382 is a kind of high performance and low power consumption bitcoin mining ASIC.

1.1 Features

- Typical hash rate and power

Voltage(V)	Hash Rate(GH/s)	Current(A)	Total power(W)	W/GH
0.72	14.18	10.40	7.49	0.528
0.75	15.75	12.24	9.18	0.583
0.80	17.33	15.20	12.16	0.702
0.85	17.33	20.00	17.00	0.981

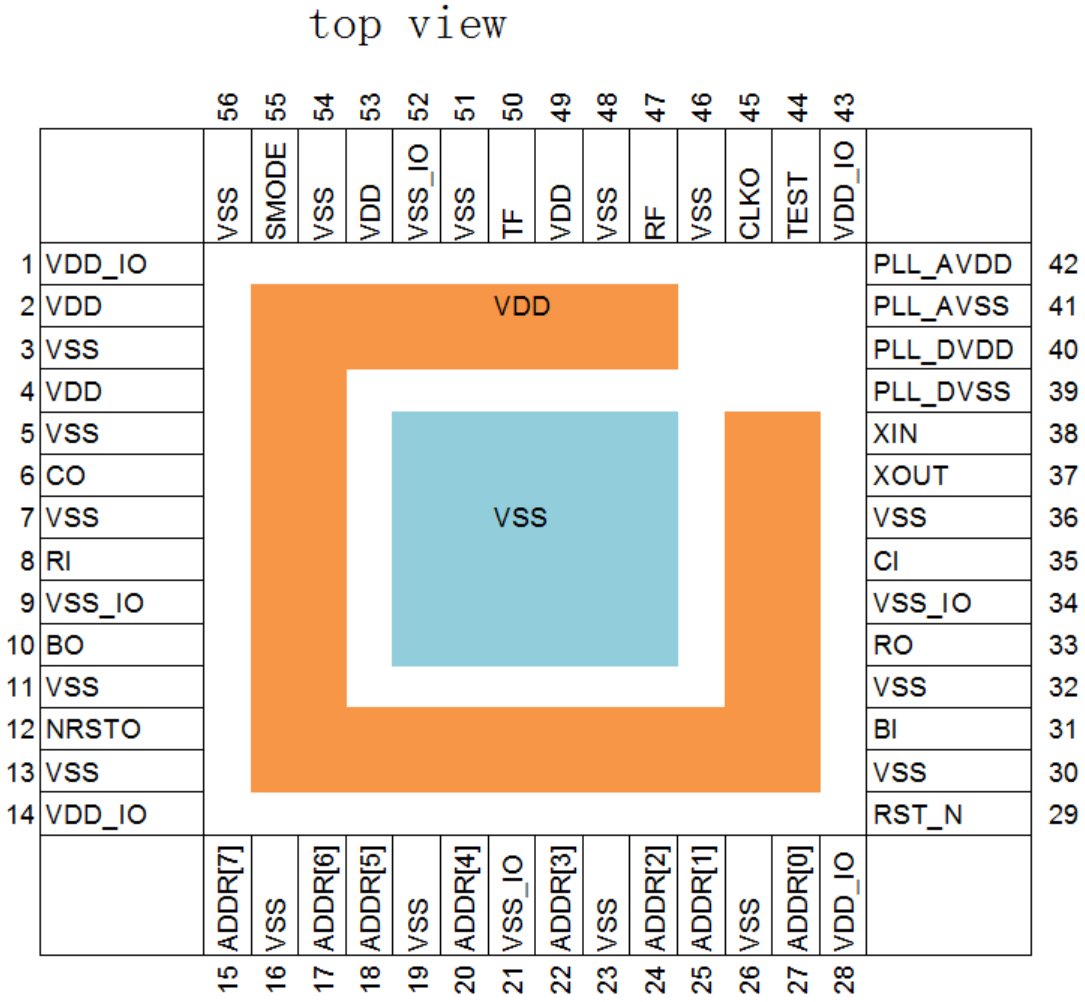
- Customized QFN56 package
- Support asynchronous UART and synchronous UART interface
- Support chain mode, Max 256 chips per chain
- Support hardware addressing and software addressing

1.2 Applications

- Bitcoin mining

2Pin Description

2.1 Pin Diagram



2.2 Signal Description

Name	I/O	Active Level	Description
XIN	I	N/A	Oscillator input
XOUT	O	N/A	Oscillator output
RST_N	I	L	Reset signal
TEST	I	N/A	Internal pull down. 0: Normal mode 1: Test mode

Name	I/O	Active Level	Description
SMODE	I	N/A	Serial Mode. Internal pull up. 0: Asynchronous UART mode. 1: Synchronous UART mode.
CLKOUT	O	N/A	Clock output
NRSTO	O	L	Reset output
CI	I	N/A	Command Input
CO	O	N/A	Command Output
RI	I	N/A	Respond Input
RO	O	N/A	Respond Output
BI	I	H	Respond Busy Input
BO	O	H	Respond Busy Output
ADDR[7:0]			Address Input. Internal pullup.
RF	O		Command Rx Flag
TF	O		Respond Tx Flag
PLL_AVDD			PLL analog power (1.8V)
PLL_AVSS			PLL analog ground
PLL_DVDD			PLL digital power (0.9V)
PLL_DVSS			PLL digital ground

3Work Input timing

Clock Freq. (M)	Hash rate (G)	Reg. value	Ideal delay (ms)	Recommend delay (ms)
100	6.30	0783	42.6	38
125	7.88	0983	34.0	31
150	9.45	0b83	28.4	26
175	11.03	0d83	24.3	22
200	12.60	0782	21.3	19
225	14.18	0882	18.9	17
250	15.75	0982	17.0	15
275	17.33	0a82	15.5	14
300	18.90	0b82	14.2	13
325	20.48	0c82	13.1	12
350	22.05	0d82	12.2	11
375	23.63	0e82	11.3	10
400	25.20	08f2	10.6	10

Programming the Output Clock Frequency

$F_{REF} = F_{IN} / NR$

$F_{VCO} = F_{OUT} * NO$

$F_{OUT} = F_{IN} * NF / (NR*NO)$, where F_{REF} is the comparison frequency for the PFD.

For proper operation in normal mode, the following constraints *must* be satisfied:

Input Divider Value (NR)

NR = 16*R[4] + 8*R[3] + 4*R[2] + 2*R[1] + R[0] + 1 = R[4:0] + 1

Feedback Divider Value (NF)

NF = 2 * (64*F[6] + 32*F[5] + 16*F[4] + 8*F[3] + 4*F[2] + 2*F[1] + F[0] + 1) = 2 * (F[6:0] + 1)

Output Divider Value (NO)

OD[1:0]	00_2	01_2	10_2	11_2
NO	1	2	4	8

Table. 4 PLL output divider setting table

High-band

$25\ MHz \le F_{REF} \le 50\ MHz$

$1500\ MHz \le F_{VCO} \le 3000\ MHz$

$187.5\ MHz \le F_{OUT} \le 3000\ MHz$

Low-Band

$10\ MHz \le F_{REF} \le 50\ MHz$

$800\ MHz \le F_{VCO} \le 1600\ MHz$

$100\ MHz \le F_{OUT} \le 1600\ MHz$

4Electrical Character

4.1 Absolute Maximum Rating

Symbol	Parameter	Max value	Unit
VDD	Core Voltage	1.2	V
VCC	IO Voltage	1.98	V
PLL_DVDD	PLL Digital power	1.2	V
PLL_AVDD	PLL analog Power	1.92	V
T_{STG}	Storage Temperature	-65~150	℃

4.2 Recommended Operation Conditions

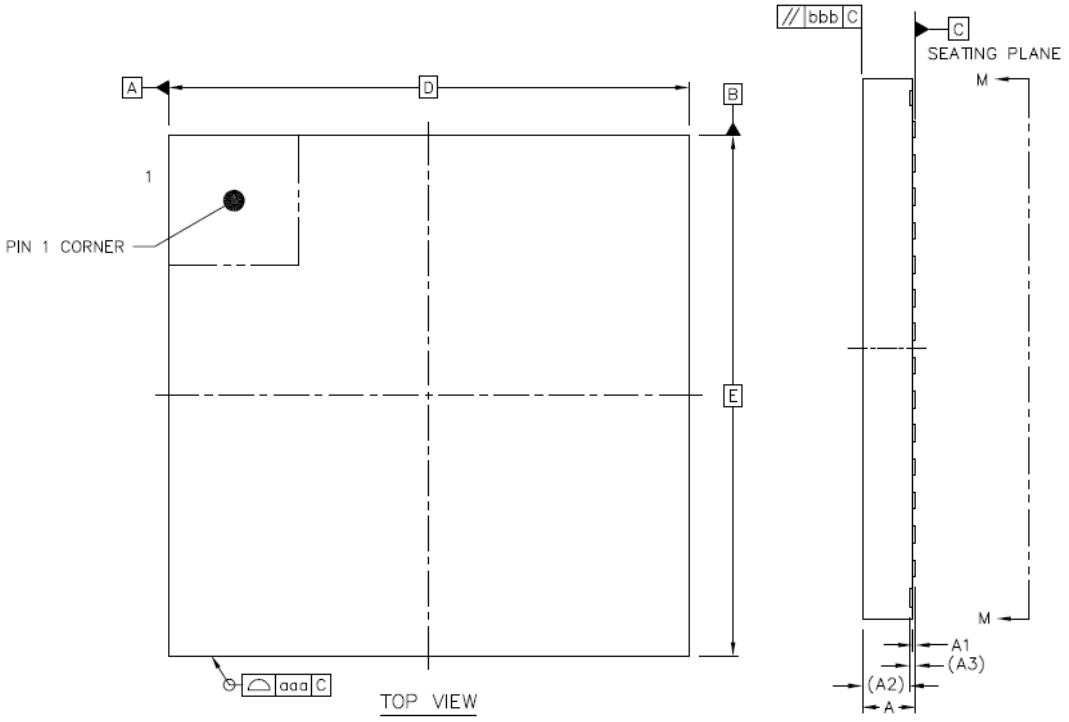
Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Voltage	0.75	0.8	1.1	V
VCC	IO Voltage	1.62	1.8	1.98	V
PLL_DVDD	PLL Digital power	0.81	0.9	0.99	V
PLL_AVDD	PLL analog Power	1.62	1.8	1.98	V
T_{OPT}	Operation Temperature	0	25	125	℃

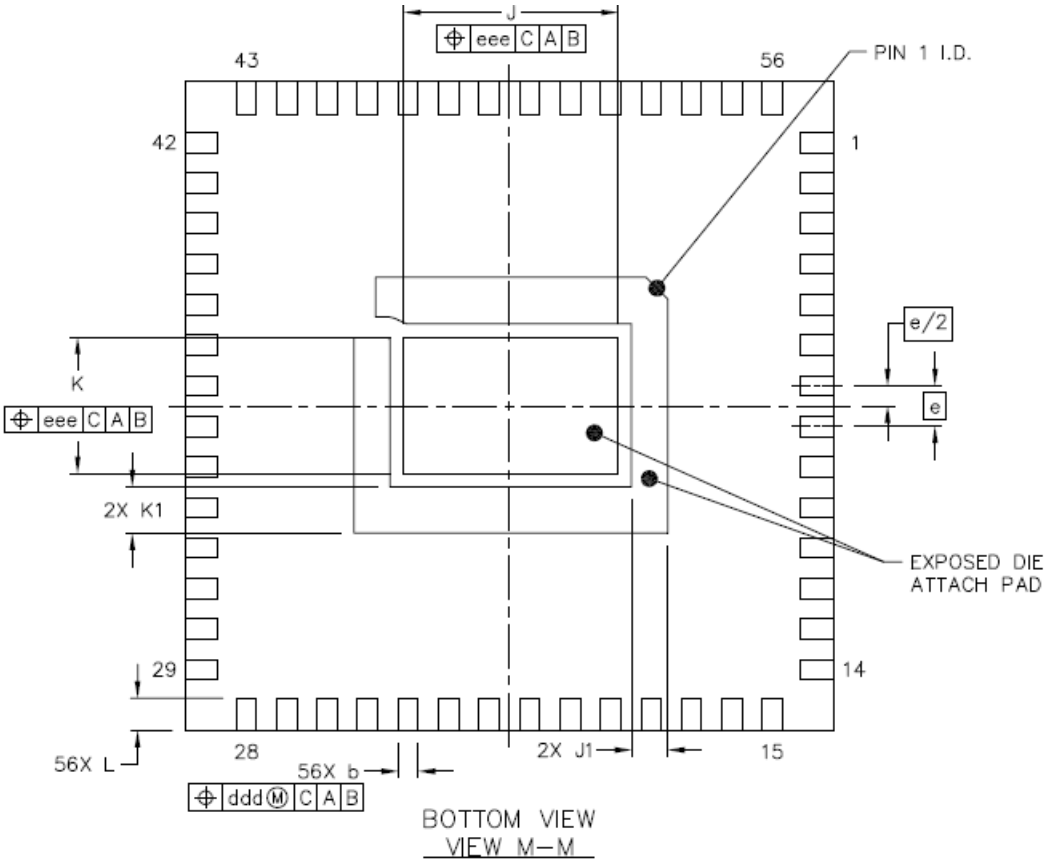
4.3 DC Characters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		1.98	V
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_L	Input Leakage Current			±10	uA
V_T	I/O threshold point	0.81	0.89	0.97	V
V_{T+}	Schmitt input low to high threshold pint	0.95	1.03	1.10	V
V_{T-}	Schmitt input high to low threshold pint	0.64	0.75	0.86	V
R_{PU}	I/O internal pull-up resistor	47K	69K	106K	Ω
R_{PD}	I/O internal pull-down resistor	49K	85K	159K	Ω
I_{CC}(VCC)	Supply current of VCC		10		mA
I_{CC}(PLL)	Supply current of PLL_DVDD and PLL_AVDD		4		mA

CB_{IN}	Input pin capacitance		10		pF
CB_{OUT}	Output pin capacitance		10		pF

5Package Outline





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.85
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2		0.7 REF	
L/F THICKNESS		A3		0.09 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	2.5516	2.6516	2.7516
		J1	0.3454	0.4454	0.5454
	Y	K	1.5814	1.6814	1.7814
		K1	0.4705	0.5705	0.6705
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.2	
LEAD OFFSET		ddd		0.08	
EXPOSED PAD OFFSET		eee		0.1	